PATENT

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REMARKS

In the Final Office Action, the Examiner noted that claims 1-20 are pending in the application. The Examiner rejected claims 1, 2, 6-9, and 13-20, and objected to claims 3-5 and 10-12. In view of the following discussion, the Applicant submits that none of the claims now pending in the application are anticipated under the provisions of 35 U.S.C. §102. Thus, the Applicant believes that all of these claims are now in condition for allowance.

I. Objections

The Examiner has objected to dependent claims 3-5 and 10-12 as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form. The Applicant thanks the Examiner for indicating allowable subject matter, but believe independent claims 1 and 8, from which these dependent claims depend, are allowable over the prior art of record for the reasons set forth below. Thus, the Applicant contends that claims 3-5 and 10-12 should distinguish over the prior art of record, since each claim depends from independent claims 1 or 8. Therefore, the Applicant respectfully requests that the objection to claims 3-5 and 10-12 be withdrawn.

II. Rejection of Claims Under 35 U.S.C. §102

The Examiner rejected claims 1, 2, 6-9, and 13-20 as being anticipated by Rahut (United States patent 6,766,504, issued July 20, 2004). The rejection is respectfully traversed.

The question for review is whether Rahut discloses determining sets of timing attributes for a routing topology of a template associated with a circuit design, where each set of timing attributes is associated with one of a plurality of locations within an integrated circuit in which the circuit design is placeable. The Examiner cited FIGs. 1A and 1B, which show a network of objects (A through G) and connections between the objects. The Examiner stated that the objects (A through G) represent a circuit design that is placeable and that sets of timing attributes are determined for independent connections between the network objects. The Examiner concluded that Rahut

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teaches determining sets of timing attributes for multiple placements of a circuit design. (Final Office Action, pp. 3-4). Applicants submit that the prima facie case of anticipation is based on clear error in interpretation of Rahut with respect to Applicant's claims.

In particular, the Examiner is conflating the circuit design shown in FIGs. 1A and 1B with the objects that comprise the circuit design. Timing attributes for multiple independent connections of a placed circuit design are not the same as timing attributes for multiple placements of a circuit design. In essence, Rahut teaches determining a single set of timing attributes for a single placement of the circuit design, where the set of timing attributes includes timing attributes for multiple independent connections. In contrast, Applicant's claim 1 recites multiple sets of timing attributes for multiple placements of the circuit design within the integrated circuit. See Applicant's claim 1, reciting "determining sets of timing attributes for the routing topology, each set of timing attributes being associated with one of a plurality of locations within the integrated circuit in which the circuit design is placeable."

There is no teaching or suggestion in Rahut that timing attributes are determined for multiple placements of the circuit design of FIGs. 1A and 1B. While Rahut discloses determining timing attributes for multiple independent connections of the circuit design, such timing attributes are only for a single placement of the circuit design. Rahut does not disclose aspects of circuit design placement within an integrated circuit, but is rather concerned with the routing phase. While the circuit design of FIGs. 1A and 1B must be placed before routing, there is no teaching or suggestion that the circuit design is placed in multiple locations within an integrated circuit and that timing attributes are determined for each such location. Rahut assumes the circuit design has been placed and then concentrates solely on the routing algorithm.

"Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim."

<u>Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.</u>, 221 USPQ 481, 485 (Fed. Cir. 1984). Since Rahut does not teach determining sets of timing attributes for respective placements of a circuit design in an integrated circuit, Rahut does not

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teach each and every element of Applicant's claim 1 as arranged therein. Accordingly, Rahut does not anticipate Applicant's invention recited in claim 1.

Independent claims 8, 15, 17, and 19 include features similar to those of claim 1 emphasized above. For the same reasons set forth above, the Applicant contends that Rahut does not anticipate the invention of claims 8, 15, 17, and 19. Finally, claims 2, 6-7, 9, 13-14, 16, 18, and 20 depend, either directly or indirectly, from claims 1, 8, 15, 17, and 19 and recite additional features therefor. Since Rahut does not anticipate Applicants' invention as recited in claims 1, 8, 15, 17, and 19, dependent claims 2, 6-7, 9, 13-14, 16, 18, and 20 are also not anticipated and are allowable.

In view of the foregoing, the Applicant contends that the interpretation of Rahut as applied to Applicant's claims is in clear error. As such, a prima facie case of anticipation has not been demonstrated as all of the claimed elements are not taught or suggested by Rahut. Applicants contend that claims 1, 2, 6-9, and 13-20 are patentable over Rahut and, as such, fully satisfy the requirements of 35 U.S.C. §102. Accordingly, the Applicant respectfully requests that the rejection of such claims be withdrawn.

CONCLUSION

Thus, the Applicant submits that none of the claims presently in the application are anticipated under the provisions of 35 U.S.C. §102. Consequently, the Applicant believes that all these claims are presently in condition for allowance. Accordingly, both reconsideration of this application and its swift passage to issue are earnestly solicited.

If, however, the Examiner believes that there are any unresolved issues requiring the maintenance of any adverse final action in any of the claims now pending in the application, it is requested that the Examiner telephone Keith A. Chanroo (408) 879-7710 so that appropriate arrangements can be made for resolving such issues as expeditiously as possible.

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All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on August 21, 2006.

Pat Tompkins

Name